CLAIMS

1	1.	. A transceiver circuit, said circuit comprising:									
2		a transmi	itter, said t	ransmit	ter transmi	tting a	norma	l link pul	se du	ring idle peri	od;
3					,					sceiver; and	
4				1	utilizing	said	clock	signals	for	minimizing	power
5	consur	nption. DA2	>								